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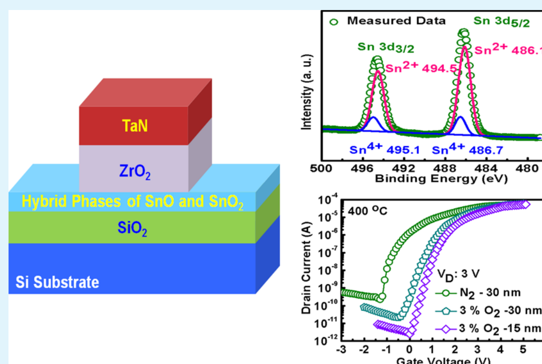
Low-Voltage Operation of ZrO_2-Gated n-Type Thin-Film Transistors Based on a Channel Formed by Hybrid Phases of SnO and SnO_2

Hsin-Chueh Chu, Yung-Shao Shen, Ching-Heng Hsieh, Jia-Hong Huang, and Yung-Hsien Wu*

Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan

ABSTRACT: With SnO typically regarded as a p-type oxide semiconductor, an oxide semiconductor formed by hybrid phases of mainly SnO and a small amount of SnO_2 with an average [O]/[Sn] ratio of 1.1 was investigated as a channel material for n-type thin-film transistors (TFTs). Furthermore, an appropriate number of oxygen vacancies were introduced into the oxide during annealing at 400 °C in ambient N_2, making both SnO and SnO_2 favorable for current conduction. By using high-κ ZrO_2 with a capacitance equivalent thickness of 13.5 nm as the gate dielectric, the TFTs processed at 400 °C demonstrated a steep subthreshold swing (SS) of 0.21 V/dec, and this can be ascribed to the large gate capacitance along with a low interface trap density (D_{it}) value of 5.16×10^{11} cm^{-2} eV^{-1}. In addition, the TFTs exhibit a relatively high electron mobility of 7.84 cm^2/V·s, high ON/OFF current ratios of up to 2.5×10^5, and a low gate leakage current at a low operation voltage of 3 V. The TFTs also prove its high reliability performance by showing negligible degradation of SS and threshold voltage (V_T) against high field stress (−10 MV/cm). When 3% oxygen annealing is combined with a thinner channel thickness, TFTs with even higher I_{ON}/I_{OFF} ratios exceeding 10^7 can also be obtained. With these promising characteristics, the overall performance of the TFTs displays competitive advantages compared with other n-type TFTs formed on binary or even some multicomponent oxide semiconductors and paves a promising and economic avenue to implement an n-type oxide semiconductor without doping for production-worthy TFT technology. Most importantly, when combined with the typical SnO-based p-type oxide semiconductor, it would usher in a new era in achieving high-performance complementary metal oxide semiconductor circuits by using the same SnO-based oxide semiconductor.



KEYWORDS: *SnO_2/SnO hybrid channel, n-type TFTs, mobility, subthreshold swing, ZrO_2, CET, interface trap density, reliability*

With the advent of a novel oxide semiconductor for an active channel layer of thin-film transistors (TFTs), flat-panel displays are a ubiquitous commodity product representing a huge market. For an n-type oxide semiconductor, several promising materials such as InGaZnO,[1,2] YInZnO,[3] SnInZnO,[4] and ZrSnZnO[5] have been extensively studied. Although good electrical characteristics have been reported, these quaternary oxide semiconductors require rigorous control of the composition and therefore add process complexity. Moreover, most of these materials necessitate the incorporation of Ga or In, which are relatively rare on earth and result in possible material shortage. To simplify process control while maintaining a desirable electrical performance, the search for an appropriate Ga/In-free binary oxide semiconductor never stops. Since its debut in 1968, crystalline ZnO, which can be prepared by radio-frequency (RF) sputtering,[6] atomic layer deposition,[7] or pulse laser deposition,[8] has attracted intensive interest and demonstrated mobility higher than 20 cm^2/V·s.[6] Unfortunately, the subthreshold swing (SS), which is crucial for device switching, is larger than 1.3 V/dec and needs further improvement. Doping ZnO with Li[9] or Ga[10] has also been explored; however, there is still room to improve the device performance. TiO_x, another widely examined material, can be prepared by approaches similar to that of ZnO. However, the mobility did not exceed 2 cm^2/V·s[11,12] until 2013, in which year an inspiring mobility higher than 20 cm^2/V·s was reported by introducing specific chemical doping in crystalline TiO_2.[13] Nevertheless, the SS is still not steep enough and the reliability performance of gate bias stress instability is not evaluated either. Interestingly, even though SnO_2 was first developed in 1964, related researches on the material were scarcely found in the literature. Pure SnO_2 prepared by RF sputtering[14] (in the crystalline phase) and spray pyrolysis[15] (in the amorphous phase) respectively showed mobilities of 2 and 0.8 cm^2/V·s along with an unsatisfactory SS, which necessitates further improvement. Furthermore, doping Sb[16] or Ta[17] into SnO_2 has been reported to have the capability of implementing n-type TFTs with significantly enhanced mobility. On the other hand, pure SnO in the crystalline phase, typically a p-type oxide semiconductor,[18] can also reveal electron transport near the conduction band minimum (CBM), and therefore SnO-based n-type TFTs were reported.[19,20] Unfortunately, the SnO-based n-type TFTs operate at large voltage and low mobilities of 1.4×10^{-3}−1.02 cm^2/V·s[19,20] with undesirable SS. In addition, these n-type TFTs behaviors were obtained from the ambipolar

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SnO conduction property rather than pure n-type devices. Even though n-type SnO can also be achieved through extrinsic doping with Sb,[21] no data for TFTs were disclosed. Furthermore, for an oxide semiconductor, nevertheless, doping the impurities[9,10,13,16,17,21] is a viable approach to boosting the field mobility of binary oxide-based TFTs by increasing the carrier concentration; it inevitably increases process costs and complexity.

Among the aforementioned n-type binary oxide semiconductors, SnO holds great potential for future flat-panel circuits because it is one of the rare materials that possess ambipolar carrier conduction behavior, which makes it possible to realize complementary metal oxide semiconductor (CMOS) circuits by a single oxide semiconductor. This implies that row and column drivers, or other peripheral circuits, can be integrated onto a glass substrate. Although the ambipolar property is attractive for simplifying circuit design and fabrication processes, challenges include the following: (a) Hole and electron mobility should be carefully controlled in ambipolar devices to obtain balanced behavior for better CMOS performance.[20] (b) There is still room to enhance its electron mobility. Nevertheless, SnO opens an opportunity to realize an n-type semiconductor. If a pure n-type rather than an ambipolar semiconductor can be realized in SnO without intentional doping, it is possible to independently optimize the performance of n-type TFTs. In combination with the typically observed SnO-based p-type semiconductor, it would usher in a new era in achieving high-performance CMOS circuits by using the same oxide semiconductor, SnO. In this work, without any doping, an oxide semiconductor composed of mainly SnO with a small amount of SnO_2 ([O]/[Sn] of 1.1) was proposed as the channel for electron transportation. Gated by ZrO_2 with a capacitance equivalent thickness (CET) of 13.5 nm, the n-type TFTs display a high electron mobility of 7.84 $cm^2/V{\cdot}s$, which outperforms undoped binary oxides such as TiO_x,[11,12] SnO_2,[14,15] SnO[19,20] and ZnO,[7,8] doped binary oxides such as LiZnO[9] and GaZnO,[10] or even InZnO-based oxides such as ZrInZnO,[2] TiInZnO[2], and YInZnO.[3] In addition, prominent electrical characteristics in terms of a large ON/OFF ratio of 2.5×10^5 and a steep SS of 0.21 V/dec, which is superior to many oxide-based TFTs,[2,3,10−12,14,15,19,20] are demonstrated. Good ZrO_2/channel interfacial quality is also proven by a low interface trap density (D_{it}) of 5.16×10^{11} cm^{-2} eV^{-1}. Furthermore, robust reliability is evidenced by the stable SS and threshold voltage (V_T) against gate bias stress. More importantly, desirable n-type TFTs can be operated at voltages as small as 3 V and implemented by a feasible and production-worthy process without doping or employing a multi-component oxide semiconductor. Considering the overall performance, the channel material composed of hybrid phases of SnO/SnO_2 along with a ZrO_2 dielectric holds competitive advantages for TFT technology.

Silicon (Si) substrates topped by SiO_2 were used as the starting materials for front-gate n-type TFTs. A 30-nm-channel material was deposited on SiO_2 by evaporating the SnO_2 source at room temperature. Subsequently, thermal annealing at 400, 450, or 500 °C was carried out for 20 min in ambient N_2 at atmospheric pressure to form the channel material. Then, 60 nm high-κ ZrO_2 was selectively deposited by e-beam evaporation as the gate dielectric. Finally, the n-type TFTs with an effective W (width)/L (length) of 120 μm/40 μm were completed by depositing TaN as the electrode followed by N_2 annealing at 300 °C. Besides electrical characterization of current−voltage (I−V), capacitance−voltage (C−V), and conductance−voltage (G−V) measurements, the effect of gate bias stress on the electrical parameters was also evaluated. The carrier concentration of the oxide semiconductor was characterized by Hall-effect measurement. In addition, physical analysis such as ex situ X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) measurement were respectively adopted for characterization of the oxide film crystallinity and bonding structure. XPS has been widely adopted in the elemental quantification,[22−24] and an accuracy of 5% is typically quoted for routinely performed XPS atomic concentrations in our XPS experimental equipment. The surface morphology of the channel material was characterized by atomic force microscopy (AFM) in separate experiments, while the dopant distribution across the oxide film was measured by secondary-ion mass spectrometry (SIMS).

Figure 1a shows the XRD spectra for a deposited SnO film annealed at 400 and 500 °C. For the 400 °C annealed film,

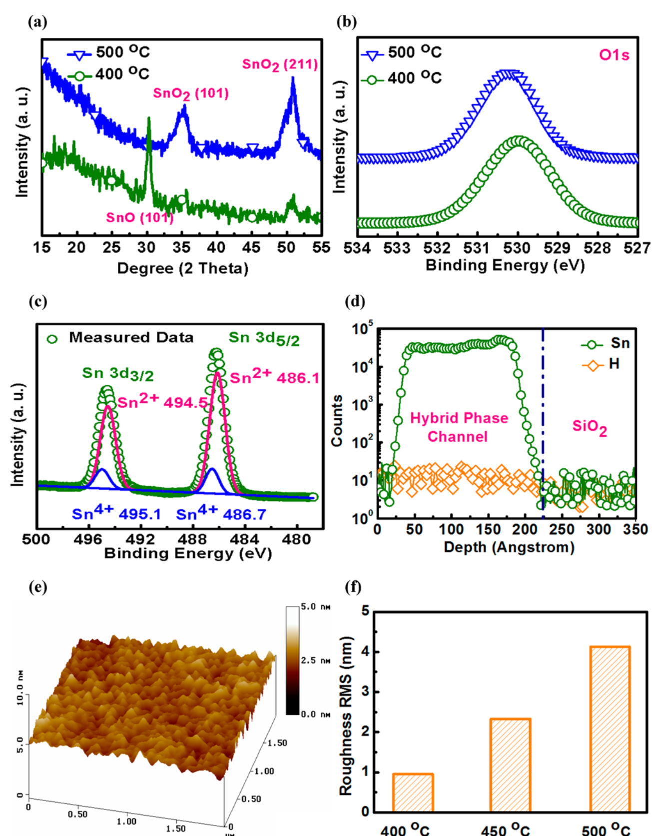

Figure 1. (a) XRD and (b) XPS O 1s spectra for 400 and 500 °C annealed SnO films. (c) XPS Sn 3d spectrum and deconvolution result for the deposited SnO film annealed at 400 °C. (d) SIMS profiles of tin and hydrogen across the 400 °C annealed SnO film. (e) AFM surface image of a 400 °C annealed SnO film. (f) AFM rms roughness values of the SnO film with various annealing temperatures.

there is a significant diffraction peak at 30.3° with some minor signals at 35.6° and 51.0°, which respectively correspond to SnO (101), SnO (101), and SnO_2 (211), suggesting a crystalline structure of the film after annealing. From the phase diagram of SnO_2, the coexistence of SnO_2 and SnO phases is possible, and it is inferred that the film is mainly composed of SnO because of the relatively strong signal in the spectrum. As the annealing temperature elevates to 500 °C, the

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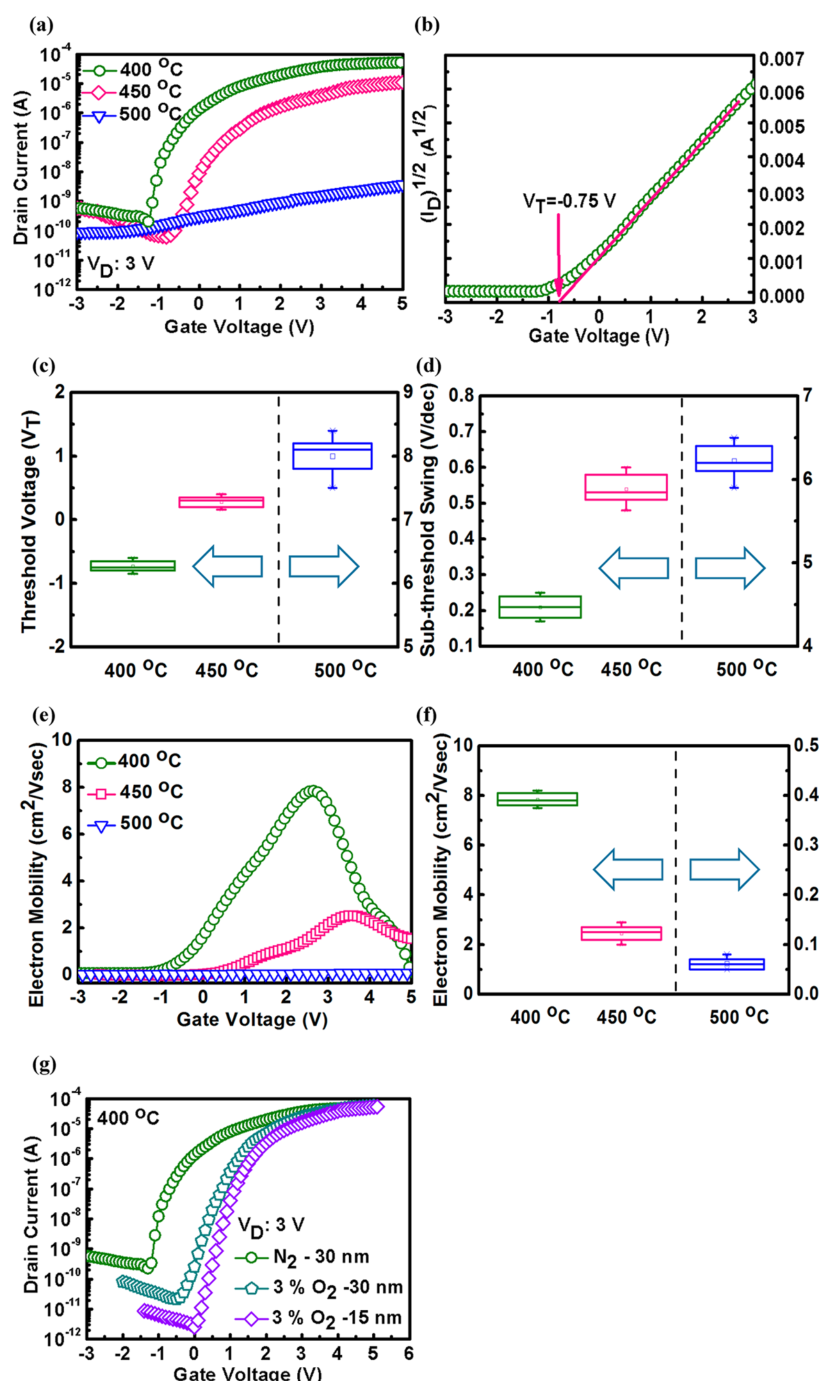

Figure 2. (a) I_D−V_G transfer characteristics with drain biased at 3 V for TFTs with the channel material annealed at various temperatures. (b) $I_D^{1/2}$−V_G curve for TFTs processed at 400 °C. Dependence of the annealing temperature of TFTs channel material on (c) statistical variation of the threshold voltage, (d) statistical variation of the SS, (e) mobility−gate voltage characteristics, and (f) statistical variation of the peak mobility. (g) Impact of annealing ambient and channel thickness on I_D−V_G transfer characteristics for TFTs with the channel material annealed at 400 °C.

signal intensity of SnO_2 significantly increases while that of SnO decreases, and this implies that SnO_2 is the main composition of the film. The phenomenon is consistent with that reported in ref 18 and can be explained by the disproportionation reaction (SnO → SnO_2 + Sn) that causes the decomposition of SnO to SnO_2 at higher temperature. Shown in Figure 1b are the annealing temperature-dependent O 1s spectra from XPS analysis. As the annealing temperature increases from 400 to 500 °C, the peak binding energy (BE) shifts toward higher energy, which implies that more O atoms are incorporated in SnO, and the results are consistent with those reported in the literature.[24] The reason why 500 °C annealing incorporates more O atoms can be explained by the fact that, although the annealing was conducted in ambient N_2, there was still residual oxygen in the ambient because it was not performed in vacuum. The inference that the 400 °C annealed film is mainly composed of SnO can be further confirmed by the XPS Sn 3d spectrum for the same sample shown in Figure 1c. It has been reported that the BE peak of Sn $3d_{5/2}$ occurs at 486.1 and 486.7 eV for SnO and SnO_2, respectively. From the deconvolution results, it can be clearly observed that the spectrum consists of a main SnO peak with a BE of 486.1 eV

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with inclusion of a minor SnO_2 peak, which is consistent with the result of XRD measurement. Besides confirming the hybrid phases with SnO and SnO_2 in the oxide film, XPS analysis also verifies the oxide film with an average composition ratio [O]/[Sn] of 1.1. Note that, from the composition ratio of [O]/[Sn], density, and molecular weights of SnO_2 and SnO, the volume fraction of SnO_2 and SnO of the film is 1:9. Even though the film was deposited from the SnO_2 source, the formation of SnO can be explained by the lattice structures of SnO_2 and SnO. For SnO_2, each Sn atom has six O-atom neighbors with a Sn−O bond length of 0.206 nm. On the other hand, for SnO, only four O-atom neighbors for each Sn atom with a bond length of 0.222 nm are found. Therefore, it is likely that the SnO_2 phase can be transformed into SnO by removing O atoms and adjusting the positions of the Sn atoms.[18,25] Figure 1d displays the SIMS profile of tin (Sn) and hydrogen (H) across the 400 °C annealed SnO film. It can be observed that the amount of hydrogen in SnO is negligible and comparable with that in the underlying SiO_2 film. Figure 1e shows the AFM surface morphology for the SnO film with 400 °C annealing, which exhibits a smooth surface with a root-mean-square (rms) roughness of 0.95 nm. The smooth SnO surface is beneficial to suppressing the charge trap at the interface between the channel and gate dielectric and alleviating the roughness-induced leakage current and carrier mobility degradation.[26,27] Figure 1f demonstrates the dependence of the annealing temperature on the SnO surface roughness. As the annealing temperature increases to 500 °C, the rms roughness slightly degrades to 4.12 nm, which may be attributed to the larger grain size of the film.

With the drain voltage (V_D) and source voltage (V_S) respectively biased at 3 and 0 V, the I_D−V_G transfer characteristics for TFTs with the channel material annealed at various temperatures are shown in Figure 2a, where I_D and V_G respectively denote the drain current and gate-to-source voltage. For 400 and 450 °C annealing, devices display apparent transistor behavior with an ON/OFF current ratio up to 2.5×10^5 and 1.6×10^5, respectively. The transistor behavior significantly degrades as the annealing increases to 500 °C. No matter what the annealing temperature is, n-type TFT behavior is found, which implies that the hybrid channel is capable of electron conduction, and this phenomenon has never been reported in the literature. Although SnO has been widely perceived as a p-type semiconductor, it was also reported that CBM of SnO is mainly formed by Sn 5p orbitals and electron transport near the CBM is possible from theoretical calculation.[20] In fact, it has also been reported that p-type SnO resulted from a shallow donor complex formed by hydrogen and tin vacancies.[28] From separate experiments in this work, p-type SnO indeed can be formed by annealing in forming gas (8% H_2/92% N_2) at 400 °C. However, from Hall-effect measurement, the p-type film has a relatively high resistivity with a low hole concentration ($\sim 10^{14}$ cm^{-3}), and it requires further process optimization for TFT applications. If one can suppress hydrogen incorporation, the p-type property of SnO can be avoided. Furthermore, it is found that the SnO channel with oxygen deficiency is favorable for electron mobility.[18] As evidenced in Figure 1d, this is the case for the 400 °C annealed film in this work, where negligible hydrogen and only a trace amount of oxygen exist in the ambient N_2 annealing because of residual oxygen. That is, negligible hydrogen prevents a p-type semiconductor from occurring, while oxygen-deficient SnO in the 400 °C annealed film provides good media for electron conduction. On the other hand, oxygen vacancies (V_O) and metal-ion interstitials are found to be the main contributors for free electrons in an n-type SnO_2-based oxide semiconductor. The role that a small amount of SnO_2 in the hybrid film plays is to introduce a certain number of oxygen vacancies into the film. These oxygen vacancies will contribute to more donor states (free electrons), and therefore the hybrid channel reveals the property of an n-type semiconductor. At 450 °C annealing temperature, from the trend obtained in XRD analysis, a larger amount of SnO_2 and a smaller amount of SnO compared to that of 400 °C will be formed in the film because of disproportionation reaction. However, the change of the SnO/SnO_2 ratio could not explain the lower drive current. The most likely reason is modulation in the oxygen amount in the film, which changes the electron conduction behavior. Because of the residual oxygen in ambient N_2 annealing, a higher annealing temperature would lead to more oxygen incorporation, which would respectively deteriorate the electron conduction in SnO because the oxygen deficiency is more favorable for the mobility and decreases the electron concentration in SnO_2 because the number of oxygen vacancies reduces. As the annealing temperature increases to 500 °C, as indicated in XRD analysis, although SnO_2 becomes the main composition of the annealed film, insignificant transistor behavior is observed. This degraded performance can be ascribed to the incorporation of an even higher amount of oxygen into SnO_2, which dramatically decreases the number of oxygen vacancies and consequently reduces the electron concentration, making the film a semiconductor of high resistivity. From evolution of the electrical characteristics for different annealing temperatures, it is confirmed that the annealing temperature and the amount of oxygen incorporated into the film play an essential role in determining the device performance. The aforementioned argument that the electron concentration decreases with increasing annealing temperature can be proven by the carrier concentration obtained by Hall-effect measurement. From the measurement, the oxide semiconductor is indeed of the n-type property. At 400 °C annealing, the carrier concentration is 5.5×10^{19} cm^{-3}, and it decreases to 1.8×10^{19} cm^{-3} as the annealing temperature elevates to 450 °C. At 400 °C annealing, it seems that the number of oxygen vacancies in SnO and SnO_2 reaches an optimum level, and therefore the best performance is achieved. Furthermore, for 400 °C annealed devices, no ambipolar behavior is found in the transfer characteristic, which is much different from the reported SnO[20] and suggests better control for the off-state current. Shown in Figure 2b is the transfer curve for 400 °C annealed devices with the drain current (I_D) axis changed to $I_D^{1/2}$. V_T of −0.75 V can be extracted from the transfer curve presented in this form. Note that the negative V_T indicates that the devices are of depletion-mode TFTs, which require negative gate bias to deplete the channel electrons to turn the devices off. It is worth noting that, because many n-type oxide semiconductor TFTs are of depletion mode, designing the driving circuits such as shift and level shifters that can be operated in depletion mode would be indispensable for an oxide semiconductor-based TFT display. Recently, many promising driving circuit designs have been proposed,[29−31] and therefore this ushers in a new era to implement depletion-mode TFTs in the driving circuits. Furthermore, it has also been reported that a TFT-based inverter with an enhancement mode driver would show higher voltage gain for a depletion load than an enhancement load,[32,33] which means depletion-mode

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Table 1. Comparison of the Main Device Parameters for n-Type TFTs with Various Channel Materials

channel material	gate dielectric	mobility (cm^2/V·s)	SS (V/dec)	I_{ON}/I_{OFF}	ref
hybrid of SnO/SnO_2	ZrO_2	7.84	0.21	2.5×10^5	this work
TiInZnO	SiO_2	0.96	0.7	2.1×10^6	2015, 2
ZrInZnO	SiN_x	3.9	0.98	$\sim 10^7$	2015, 2
YInZnO	SiO_2	4.76	2.9	1.32×10^6	2013, 3
ZnO	Al_2O_3	~4	N/A	$\sim 10^7$	2009, 7
ZnO	SiO_2/SiN_x	0.97	N/A	$>10^5$	2003, 8
LiZnO	SiO_2	1.5×10^{-2}	0.24	$\sim 10^5$	2014, 9
GaZnO	Al_2O_3	1.058	~2.2	1.08×10^6	2014, 10
TiO_x	SiO_2	1.64	1.86	4.7×10^5	2009, 11
TiO_{2-x}	SiO_2	0.69	2.45	2.04×10^7	2011, 12
SnO_2	Al_2O_3/TiO_2 superlattice	0.8	~4	$\sim 10^5$	2004, 14
SnO_2	SiO_2	0.37	2	$\sim 10^6$	2014, 15
SnO	SiO_2	1.4×10^{-3}	~3.5	$\sim 10^2$	2011, 19
SnO	SiO_2	1.02	~10	$\sim 10^3$	2012, 20

devices still have certain advantages for circuit application. Figure 2c shows that the statistical variation of V_T for different annealing temperatures and V_T shifts toward the positive direction as the annealing temperature increases. In addition to typical I_D-V_G characteristics, I_D-V_G hysteresis is important as well because it is an important indicator of dielectric bulk traps and the interfacial quality between ZrO_2 and the SnO/SnO_2 hybrid channel, and the results (not shown) for different annealing temperatures show that hysteresis for 400 °C annealed devices is 0.35 V and hysteresis deteriorates with the annealing temperature. The small hysteresis of 400 °C annealed devices implies either good interfacial quality or few dielectric bulk traps. Shown in Figure 2d are the SS for devices with various annealing temperatures. With V_D biased at 3 V, the SS for 400 °C annealed devices is 0.21 V/dec, and the value degrades to 0.52 V/dec as the annealing temperature increases to 450 °C. The degradation is partly ascribed to the worse interfacial quality, as evidenced by the hysteresis value. It is worth mentioning that the steep SS of 0.21 V/dec for 400 °C annealed devices is superior to that of many binary oxide-based TFTs such as Ga-doped ZnO,[10] TiO_2,[11,12] SnO_2,[14,15] SnO,[19,20] and even InZnO-based oxides such as ZrInZnO,[2] TiInZnO[2], and YInZnO.[3] Note that the operation voltage of 3 V in this work is much lower than that of ZrInZnO,[2] TiInZnO,[2] YInZnO,[3] LiZnO,[9] TiO_x-based,[11−13] SnO_2[14,15] and ZnO[8] n-type TFTs, which require voltages higher than 20 V. The low operation voltage is primarily due to the adoption of high-κ (high dielectric constant) ZrO_2, which leads to stronger channel control from the gate. The desirable SS also leads to high electron mobility, which is shown in Figure 2e,f, mobility versus gate voltage characteristics, and statistical variation of the peak mobility for different annealing temperatured. Note that the mobility (μ) was extracted for TFTs operated in the linear region by the equation $\mu = (\partial I_D/\partial V_G)(L/W)(1/C_{ox})(1/V_{DS})$, where L and W respectively denote the channel length and width, while C_{ox} is the capacitance per unit area. For 400 °C annealed devices, by considering the gate current effect on the drain current, the mobility can be as high as 7.84 cm^2/V·s, which outperforms undoped binary oxides such as TiO_x,[11,12] SnO_2,[14,15] SnO,[19,20] and ZnO,[7,8] doped binary oxides such as LiZnO[9] and GaZnO,[10] or even InZnO-based oxides such as ZrInZnO,[2] TiInZnO[2], and YInZnO.[3] Note that the reported mobility for n-type SnO ranges from 1.4×10^{-3} to 1.02 cm^2/V·s,[19,20] which may arise from the relatively oxygen-rich nature of the oxide film.[20] Table 1 summarizes the main electrical characteristics of n-type TFTs formed on various channel materials. Considering the overall performance and process complexity, the SnO/SnO_2 hybrid channel gated by the ZrO_2 dielectric indeed holds the potential to realize high-performance TFTs in a more economic approach. Note that a high ON/OFF current ratio is desirable for TFT devices and there is still room to enhance the ratio of 400 °C annealed devices. In fact, from separate experiments, the mechanical stress between ZrO_2 and SnO is measured to be −0.04 GPa from a laser curvature method, which is based on variation of the characteristic curvature radius of the sample before and after ZrO_2 deposition. The stress is so small that it is not the main reason for the unsatisfactory ON/OFF current ratio. The most likely reason is the high OFF-state current (I_{OFF}), which may have resulted from the following factors.

1. HIGH CONDUCTIVE CHANNEL

The channel contains a large number of oxygen vacancies and, consequently, a high carrier concentration in the channel material. It is the high carrier concentration that makes the device difficult to be completely depleted, and therefore high I_{OFF} is observed. By moderation of the number of oxygen vacancies in the channel through additional annealing in oxygen-containing ambient such as wet air,[34] further improved I_{OFF} may be achieved. From our preliminary experimental results, as shown in Figure 2g, by annealing the channel material at 400 °C in N_2 ambient with 3% oxygen, the TFTs demonstrated I_{OFF} of 2.1×10^{-11} A/cm^2, which is lower than that from N_2 annealing at the same temperature by nearly 1 order of magnitude, with the ON-state current (I_{ON}) kept almost unchanged. Therefore, the I_{ON}/I_{OFF} ratio enhances to 2.8×10^6. Although there is still room to further improve the ratio, annealing the channel material in oxygen-containing ambient indeed provides an alternative direction. A more in-depth study in this direction will be reported elsewhere. Besides the reduced I_{OFF}, the other important observation is that devices annealed in the ambient with 3% oxygen incorporation also display a positive V_T shift from −0.75 to 0.88 V, indicating the change of the operation mode from depletion to enhancement, which would provide more flexibility in circuit design. The behavior of I_{OFF} reduction as well as the change of the operation mode can be explained by modulation of the number of oxygen vacancies in the channel.

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2. HIGH GATE LEAKAGE CURRENT

It has been reported[35] that, for depletion-mode TFTs, I_{OFF} includes not only leakage from the channel, as mentioned in part 1, but also the gate leakage current. In this work, the gate leakage current for 400 °C annealed TFTs at −1 V is comparable with the drain current at the same bias and it indeed has room to suppress the gate leakage to improve I_{OFF}. Further reduced gate leakage current is expected by adopting appropriate surface passivation for the hybrid channel to enhance the bonding structure between ZrO_2 and the channel material and employing additional annealing on ZrO_2 to strengthen the bonding structure in the oxide bulk.

3. THICK CHANNEL MATERIAL

High I_{OFF} is observed if the channel is difficult to deplete. Besides the high carrier concentration of the channel, the relatively thick channel thickness also makes the channel difficult to completely deplete,[32] which is the case in this work because the channel thickness is 30 nm. On the basis of the aforementioned result that TFTs processed at 400 °C in ambient N_2 with 3% oxygen exhibit a better I_{ON}/I_{OFF} ratio than pure N_2 annealing, devices with the same annealing conditions but with a thinner channel thickness of 15 nm were fabricated and investigated. The I_D-V_G transfer characteristic was demonstrated in Figure 2g. As expected, compared to those with a channel thickness of 30 nm, devices with a 15 nm channel thickness exhibit lower I_{OFF}, comparable I_{ON}, and higher I_{ON}/I_{OFF} ratio of 2.2×10^7. The improved I_{ON}/I_{OFF} ratio for the decreased channel thickness can be explained by the reduced bulk conduction and therefore lower I_{OFF}, which is consistent with the results reported in the literature.[32,36,37] In addition, a positive shift of V_T can also be observed for those with thinner channel thickness. Given that the free electron concentration is constant in the channel layer with different thicknesses, the total number of free electrons is proportional to the channel thickness. For devices with thinner channel thickness, the decreased number of free electrons requires a less negative bias to turn off the drain current in TFTs,[32] and therefore the positive shift of V_T is obtained.

From the aforementioned physical and electrical characteristics, the competitive advantages of the hybrid phase SnO channel over other n-type oxide semiconductor TFTs are summarized below. (1) From a process point of view, the hybrid phase channel is based on a binary oxide without doping or employing a multicomponent oxide semiconductor that simplifies the process complexity and makes it a production-worthy process. (2) From an electrical performance point of view, the n-type ZrO_2-gated hybrid phase TFTs reveal advantages over previous studies in terms of a small operation voltage of 3 V, which is much lower than those reported in the literature, a higher electron mobility of 7.84 $cm^2/V{\cdot}s$, which outperforms most binary oxide semiconductor-based TFTs reported in the literature, a low SS of 0.21 V/dec, which is superior to most oxide semiconductor-based TFTs because of the employment of a high-κ dielectric. (3) From a circuit application point of view, the operation mode of the hybrid phase devices can be modulated from the depletion mode with annealing in ambient N_2 to the enhancement mode with annealing in ambient N_2 incorporated with 3% oxygen, both at 400 °C annealing. The results are very promising for circuit application because it is possible to fabricate both depletion and enhancement mode devices on the same wafer to implement inverters, with the enhancement one for the driver and the depletion one for the load. As aforementioned statements, the circuit configuration would result in a larger voltage gain than the enhancement load. That is, the hybrid phase channel proposed in this work exhibits the possibility of forming n-type depletion mode TFTs and n-type enhancement mode TFTs through appropriate annealing. Even though the latter devices are not comprehensively investigated, the hybrid phase channel indeed holds great potential to provide available choices for actual device and circuit integration.

Compared to other oxide semiconductor TFTs, the much improved mobility of the TFT channel material processed at 400 °C in this work can be attributed to the good current conduction media of the oxide film and the steep SS. The former resulted from the oxygen-deficient oxide film that makes both SnO and SnO_2 favorable for current conduction, while the latter can be ascribed to the large gate capacitance and low D_{it} between ZrO_2 and the hybrid channel. The large gate capacitance can be confirmed by the $C-V$ measurement, which is shown in Figure 3a, while low D_{it} is proven by the $G-V$ characteristic measured at 100 kHz, which is shown in Figure 3b. Figure 3a exhibits the $C-V$ curves measured at different frequencies ranging from 10 to 1000 kHz. For the $C-V$ measurement, alternating-current impedance between the gate and source was measured by applying a small signal voltage with a sweep voltage on the gate terminal. Because the gate terminal is positively biased, TFT is under the accumulation region and the measured capacitance is C_{ox} in series with C_B, where C_{ox} is the capacitance from the gate dielectric while C_B is the capacitance due to gate voltage−responsive total charge in the active film. Because C_B is much larger than C_{ox}, the measured capacitance under accumulation is mainly determined by C_{ox}.[38] A maximum capacitance occurring at the positive gate voltage suggests that the hybrid channel has n-type semiconductor nature. From the measured capacitance at a gate voltage of 3 V with a measurement frequency of 100 kHz, the

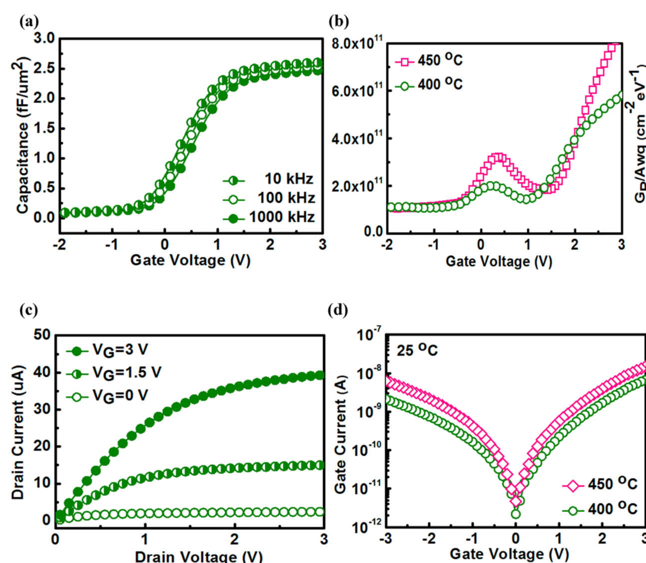

Figure 3. Electrical characteristics for TFTs with channel material annealed at 400 °C. (a) $C-V$ curves measured at different frequencies. (b) $G-V$ curve obtained at 100 kHz. (c) I_D-V_{DS} output characteristics. (d) Gate leakage performance for the same device measured at 25 °C. $G-V$ and gate leakage for TFTs processed at 450 °C are also shown in parts b and d.

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CET of annealed ZrO_2 was extracted to be 13.5 nm with a κ value of 17.3. In addition, the small frequency dispersion in the depletion region implies the desirable interfacial quality between the dielectric and hybrid channels. From the $G-V$ characteristic shown in Figure 3b, the interfacial quality can be further quantified by the D_{it} value of 5.16×10^{11} cm^{-2} eV^{-1}, which means the trap density per unit energy in the band gap of the channel material, and it can be estimated from the peak value in the $G-V$ curve by the formula $D_{it} \sim 2.5G_{p,max}/A\omega q$, where G_p, A, and ω respectively denote the parallel conductance peak, device area, and angular frequency.[39] In fact, from the SS value, the total trap density (N_t), which includes both the density of deep bulk states in the channel (N_{bulk}) and interface states between the channel/gate dielectric (N_{it}), can also be extracted by the formula $N_t = N_{bulk} + N_{it} = [\mathrm{SS}\ \log(e)q/k_BT - 1](C_{ox}/q)$, where e is Euler's number (irrational constant), k is the Boltzmann constant, T is the absolute temperature, and q is the charge of an electron.[40] From the measured data, N_t is found to be 3.92×10^{12} cm^{-2}. There is still room to reduce the N_t value to achieve a higher device performance. For interface states, it can be further improved by adopting appropriate surface passivation for the hybrid channel or additional thermal treatment to enhance the bonding structure between ZrO_2 and the channel material. For bulk states in the channel, assuming that the trap density per area is constant, it may be improved by using a thinner channel thickness, which is still under investigation. Also shown in Figure 3b is the $G-V$ characteristic for TFTs processed at 450 °C. From the peak value, its D_{it} is extracted to be 8.52×10^{11} cm^{-2} eV^{-1}, which is higher than that of 400 °C annealed TFTs and may arise from a rougher surface. The higher D_{it} value is consistent with the larger hysteresis, and it also partly explains the worse SS performance and inferior mobility. Figure 3c displays the output characteristics for devices with 400 °C annealing. The devices demonstrate obvious pinch-off voltage and current saturation. It can be clearly seen that the operating voltage can be as low as 3 V, which is essential for green electronics. Figure 3d shows the gate current (I_G)$-V_G$ curve measured at 25 °C for TFTs processed at 400 and 450 °C. At V_G of 3 V, which corresponds to the ON state, a gate leakage current of 1.4×10^{-8} A is obtained for 450 °C annealed TFTs, and the current improves to 6.8×10^{-9} A as the annealing temperature lowers to 400 °C. The improved leakage current performance can be ascribed to lower D_{it} and a smoother dielectric/channel interface. Obviously, the current at positive bias is higher than that at negative bias. The asymmetric current level for different bias polarities also implies the n-type semiconductor property of the channel because it is under the accumulation regime at positive bias.

Besides understanding the electrical behavior of the ZrO_2-gated TFTs formed on the SnO/SnO_2 hybrid channel, reliability assessment for the devices is important as well to ensure its feasibility for practical applications. Related reliability assessment conducted under ON and OFF states was studied. Because bias stress in the dark environment is not a significant issue, therefore the reliability under illumination either for a positive or a negative gate bias was also evaluated. To address the issue, with V_D fixed at +6 V, V_G of −13.5 and +13.5 V are respectively applied on the gate to evaluate its V_T instability under OFF (negative bias stress, NBS) and ON (positive bias stress, PBS) states in the dark environment. For assessment of the negative bias illumination stress (NBIS) and positive bias illumination stress (PBIS), a blue-light-emitting diode with a wavelength of 430 nm and a power density of 0.1 mW/cm^2 was adopted for the reliability test. Parts a and b of Figure 4 respectively demonstrate the NBS/PBS and NBIS/PBIS results for 400 °C annealed devices. The V_T shift for NBS is −0.49 V after 10^4 s of stress, and the data are comparable with those for PBS. The results confirm that V_T instability is not a critical issue in the dark environment. In contrast, under the illumination of blue light, the V_T shift for NBIS degrades to −1.29 V after 10^4 s of stress, while the result for PBIS becomes slightly better than PBS after the same stress. The remarkable difference between NBIS and PBIS can be explained as follows. In the hybrid phase channel, oxygen vacancies (V_O) locate in the band gap of the SnO film. Under illumination, because of the high photoenergy from blue light, electrons in the valence band maximum (VBM) can be excited to the energy states of the V_O, and the process leaves holes at the VBM. Because the negative bias continues to apply on the gate, the induced holes will be trapped at the interface between the gate dielectric and channel material and/or the bulk region of the gate dielectric because of the favorable electric field and consequently band bending.[41] As the amount of trapped holes increases, V_T shift toward the negative direction can be observed. For PBIS, the slightly improved V_T shift compared to that of PBS can be ascribed to electron derapping from the gate dielectric with illumination and therefore the V_T shift becomes less pronounced.[42]

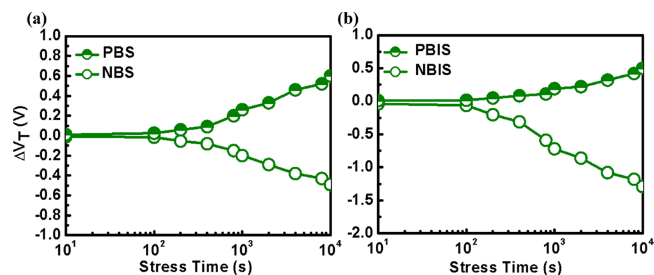

Figure 4. Impact of the gate bias stress time on V_T instability with a high gate voltage of ±13.5 V under (a) dark and (b) illumination environments measured at 25 °C.

In conclusion, an undoped oxide semiconductor with hybrid phases of SnO/SnO_2 was explored as the channel material for n-type TFTs. At 400 °C annealing, the channel is composed of a small amount of SnO_2 inclusion in the SnO film, and an optimum number of oxygen vacancies were introduced into the oxide film, making both SnO and SnO_2 favorable for current conduction. Several promising electrical characteristics in terms of a high electron mobility of 7.84 cm^2/V·s, a steep SS of 0.21 V/dec, a large ON/OFF current ratio up to 2.5×10^5, a small D_{it} value of 5.16×10^{11} cm^{-2} eV^{-1}, and a low gate leakage current were obtained for the ZrO_2-gated TFTs operated at a voltage of 3 V. Upon integration of 3% oxygen annealing with a thinner channel thickness, TFTs with even higher I_{ON}/I_{OFF} ratios exceeding 10^7 can also be obtained. A good reliability performance is also evidenced by the relatively stable SS and V_T under high voltage stress. Compared to other n-type oxide semiconductors, the overall performance of the undoped hybrid channel devices suggests that it holds the potential to empower advanced low-power/high-performance TFTs. Most importantly, the hybrid channel proves the feasibility to achieve high electron mobility in a SnO-based oxide semiconductor and paves a possible avenue to implement depletion/enhancement TFTs and even CMOS TFTs by a single material.

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AUTHOR INFORMATION

Corresponding Author

*E-mail: yunhwu@mx.nthu.edu.tw.

Author Contributions

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Notes

The authors declare no competing financial interest.

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